

In the Claims:

Please amend claims 2-3, 7-9, 11-12, 14 and 16-18, cancel claims 6 and 15, and add new claims 19 and 20 as indicated below. This listing of claims replaces all prior versions.

1. *(Cancelled)*

2. *(Currently amended)* As A bus system as claimed in claim 3, wherein the output means comprises a multiplexer operably connected to receive the first and second output signals, and operable to output the receiver output signal in dependence upon a previous receiver output signal.

3. *(Currently amended)* A bus system for an integrated circuit device, the bus comprising a plurality of bus lines each of which connects a driver circuit and a receiver circuit; and a glitch sensor circuit which is operable to detect glitches on at least one of the bus lines, characterized in that each receiver circuit comprises:

a first detector operably connected to receive a data signal from an associated bus line, and operable to detect a rising transition of the data signal with respect to a first threshold level, and to produce a first output signal upon detection of such a rising transition;

a second detector operably connected to receive the data signal, and operable to detect a falling transition of the data signal with respect to a second threshold level, and to produce a second output signal upon detection of such a transition;

output means operable to output the first or second output signal as a receiver output signal; and

wherein the first and second threshold levels are variable.

4. *(Previously Presented)* A bus system as claimed in claim 3, further comprising a calibrator for adjusting the first and second threshold levels.

5. (*Previously Presented*) A bus system as claimed in claim 4, wherein the first and second detectors include respective pluralities of transistors, and the calibrator is operable to activate varying numbers of those transistors, in order to adjust the threshold levels.
6. (*Cancelled*) A bus system as claimed in claim 4, further comprising a glitch sensor circuit which is operable to detect glitches on at least one of the bus lines.
7. (*Currently amended*) A bus system as claimed in claim 4 [[6]], wherein the glitch sensor circuit comprises a pair of latches each having an output, and a multiplexer operable to select one of the latch outputs for supply to the calibrator.
8. (*Currently amended*) A bus system as claimed in claim 4 [[6]], wherein the calibrator is operable to supply test signals to the bus lines, and the glitch sensor circuit is operable to detect glitches on at least one bus line and to supply a glitch signal to the calibrator, the calibrator then being operable to adjust the threshold values of the detectors in dependence upon the glitch signal.
9. (*Currently amended*) A bus system as claimed in claim 4 [[6]], further comprising a test bus including a plurality of test drivers, and corresponding pluralities of bus lines and receivers, the calibrator being operable to supply test signals to the test bus lines, and the glitch sensor circuit being operable to detect glitches on the test bus lines and to supply a glitch signal to the calibrator, the calibrator then being operable to adjust the threshold values of the detectors in dependence upon the glitch signal.
10. (*Cancelled*)
11. (*Currently amended*) A method as claimed in claim 12, wherein the first or second output signal is output by a multiplexer operably connected to receive the first and second output signals, and operable to output the receiver output signal in dependence upon a previous receiver output signal.

12. (*Currently amended*) A method of operating a bus system for an integrated circuit device, the bus comprising a plurality of bus lines each of which connects a driver circuit and a receiver circuit, characterized in that the method comprises:

receiving a data signal from a bus line;

detecting a rising or falling transition of the data signal with respect to first and second threshold levels respectively, wherein the first and second threshold levels are variable;

producing a first output signal upon detection of a rising transition, or producing a second output signal upon detection of a falling transition; and

outputting the first or second output signal as a receiver output signal; and

detecting glitches on at least one of the bus lines.

13. (*Original*) A method as claimed in claim 12, further comprising adjusting the first and second threshold levels.

14. (*Currently amended*) A method as claimed in claim 13, wherein the rising transition is detected by a first detector and the falling transition is detected by a second detector, the first and second detectors include respective pluralities of transistors, and the threshold levels are adjusted by activating varying numbers of those transistors.

15. (*Cancelled*) A method as claimed in claim 13, further comprising detecting glitches on at least one of the bus lines.

16. (*Currently amended*) A method as claimed in claim 12 [[15]], wherein the glitches are sensed using a glitch sensor circuit which comprises a pair of latches each having an output, and a multiplexer operable to select one of the latches.

17. (*Currently amended*) A method as claimed in claim 12 [[15]], further comprising supplying test signals to the bus lines, detecting glitches on at least one bus line, and adjusting the threshold values in dependence upon the detected glitches.

18. (*Currently amended*) A method as claimed in claim 12 ~~[[15]]~~, further comprising supplying test signals to test bus lines, detecting glitches on the test bus lines, and adjusting the threshold values in dependence upon the detected glitches.

19. (*New*) A bus system as claimed in claim 3, wherein the glitches are signals on one of the bus lines caused by crosstalk from data signals on the other bus lines, the glitches causing transitions to be detected by at least one of the first and second detectors associated with the one of the bus lines.

20. (*New*) A method as claimed in claim 12, wherein the glitches are signals on one of the bus lines caused by crosstalk from data signals on the other bus lines, the glitches causing transitions to be detected by at least one of the first and second detectors associated with the one of the bus lines.